

## ABSTRACT:

To provide a circuit arrangement (100) for controlling a first terminal and a second terminal of a preferably contactless integrated circuit, particularly for testing a CMOS circuit, with which a multitude of integrated circuits can be tested simultaneously while using a low-cost structure and by which the circuit arrangement for a simple write/read unit assigned to the integrated circuit can be provided, it is proposed that the circuit arrangement (100) comprises:

- at least a control stage (10) which generates, from an external modulation signal ( $M_0$ ) and an external clock signal ( $C_0$ )
  - a first modulation signal ( $M_1$ );
  - a second modulation signal ( $M_2$ ) which is temporally shifted with respect to the first modulation signal ( $M_1$ );
  - a preferably symmetrical first clock signal ( $C_1$ ); and
  - a preferably symmetrical second clock signal ( $C_2$ ) which is inverted with respect to the first clock signal ( $C_1$ );
- at least a first driver stage (40),
  - which is connected to a first power supply voltage ( $U_{dd,1}$ ) amplitude-modulated by the first modulation signal ( $M_1$ ) and to a first reference potential ( $U_{ss,1}$ ) and
  - can be impressed with the first clock signal ( $C_1$ ) in such a way that the output voltage ( $U_{o,1}$ ) of the first driver stage (40), which can be applied to the first terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated first power supply voltage ( $U_{dd,1}$ ) and temporally the value of the first reference potential ( $U_{ss,1}$ ) in accordance with the clock of the first clock signal ( $C_1$ ); and
- at least a second driver stage (50),
  - which is connected to a second power supply voltage ( $U_{dd,2}$ ) amplitude-modulated by the second modulation signal ( $M_2$ ) and to a second reference potential ( $U_{ss,2}$ ) and

- 5      -      can be impressed with the second clock signal ( $C_2$ ) in such a way that the output voltage ( $U_{o,2}$ ) of the second driver stage (50), which can be applied to the second terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated second power supply voltage ( $U_{dd,2}$ ) and temporally the value of the second reference potential ( $U_{ss,2}$ ) in accordance with the clock of the second clock signal ( $C_2$ ).

Fig. 1

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